A 32-GHz Solid-State Power Amplifier for Deep Space Communications

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A 1.5-W solid-state power amplifier (SSPA) has been demonstrated as part of an effort to develop and evaluate state-of-the-art transmitter and receiver components at 32 and 34 GHz for future deep space missions. Output power and efficiency measurements for a monolithic millimeter-wave integrated circuit (MMIC)-based SSPA are reported. Technical design details for the various modules and a thermal analysis are discussed, as well as future plans.

I. Introduction

The Deep Space Network is developing telecommunication capability at 32 GHz (Ka-band) with expected improvement of as much as 8 dB over the current performance at 8 GHz (X-band). A proof-of-concept 32-GHz solid-state power amplifier (SSPA) with an output power of 1.56 W has been designed and demonstrated for future spacecraft applications.

The objective was to demonstrate useful RF output power of greater than 1.5 W with an efficiency greater than 15 percent at 32 GHz. We also wanted to use state-of-the-art components that were readily available from vendors and to build a compact system that could be interfaced with the deep space transponder.

The development of this SSPA provided practical hands-on experience in the incorporation of Ka-band monolithic millimeter-wave integrated circuits (MMICs) into an amplifier architecture. Other useful information was obtained in the areas of mechanical and electronic system integration and high-power RF testing. The completed hardware from this effort is currently being used as a stepping stone toward 32-GHz SSPAs having higher efficiencies (>25 percent) and output power capacity (1.7 W).

II. Subsystem Design

Some initial goals and requirements for the 32-GHz SSPA were established based upon future deep space mission requirements. An RF output power level of 1.5 W having greater than 15 percent power added efficiency was selected, which would make the SSPA a good candidate for insertion into the Pluto Fast Flyby mission. The SSPA would also require 31 dB of RF gain in order to interface with the deep space transponder that provides 1 mW of input power to the SSPA.

We surveyed industry to find 32-GHz high-power devices (>0.5 W) having efficiencies greater than 25 percent in order to meet these requirements and came up with three possible vendors. GE Aerospace has 1.0-W 32-GHz pseudomorphic high electron-mobility transistor (PHEMT) discrete devices with 30 percent power added efficiency, but these were not available for use outside of GE Aerospace. Raytheon initially claimed to have

0.5-W PHEMT devices with 30 percent power added efficiency; however, sample parts only delivered 0.4 W and fell short of our requirements. Alpha has 0.5-W metal-semiconductor field effect transistor (MESFET) MMIC devices having 25 percent power added efficiency and 11-dB gain, which were available for immediate purchase. We selected the Alpha AA035-P2 0.5-W MMIC as our power amplifier component.

A. SSPA Architecture

The output from the MMICs can be combined in different ways to meet the 1.5-W output power requirement. Several architectures for the SSPA were considered, but the topology shown in Fig. 1 provided the best performance in terms of gain and power added efficiency, and used the fewest number of parts (based on the parts available at that time). The output stage for the SSPA consists of four 0.5-W power amplifier MMICs (Alpha AA035-P2) where the outputs of these four devices are combined in a corporate, in-phase, Gysel [1] microstripline combiner. The input signal to the SSPA is amplified by a preamplifier MMIC (Alpha AA035-P3) followed by a high-power driver MMIC (Alpha AA035-P2) and split through a four-way Gysel microstripline divider to feed each of the four output stages. A further consideration in determining the optimal architecture is the distribution of gain through the cascaded chain. Our SSPA design ensured that each amplifier would enter gain compression at the same unit input drive level. If the driver amplifier were to saturate before the output stages, the desired output power would not be achieved. Table 1 shows the gain distribution and efficiency calculation for this 1.5-W RF amplifier architecture, and Fig. 1 shows the associated block diagram.

The mechanical interfaces were determined by considering the other system components (transponder and antenna) as well as performance and overall size. A waveguide provides the lowest loss, and minimizing the loss (especially at the output) is important in maximizing the efficiency at the expense of larger size. The transponder output port is a coaxial connector, and the antenna input port is a waveguide. At both the input and output of the SSPA, a transition from waveguide to microstrip is required. At the input, a transition from coax to waveguide is required to mate to the transponder.

B. MMIC Amplifiers

The preamplifier MMIC (Alpha AA035-P3, the first device in the chain) provides over half the RF gain of the SSPA (17.9 dB). The frequency response and return loss plot for the preamplifier is shown in Fig. 2. This MMIC contains three identical cascaded MESFET stages with associated matching and bias circuitry to operate from a single supply, all on a single 3.9-mm by 1.9-mm chip.

The power amplifier MMICs and driver amplifier MMIC (Fig. 3) each deliver 0.5 W of RF power. The frequency response and return loss plot for an individual MMIC power amplifier is shown in Fig. 4. The output power and power added efficiency for this power MMIC is shown in Fig. 5, while the corresponding gain compression curve is shown in Fig. 6. This chip contains an input stage of two MESFETs in parallel, each driving two of the four MESFETs that make up the output stage. Power dividers, interstage matching networks, and bias networks are all integrated onto the 3.9-mm by 3.1-mm chip.

An important design criterion when combining amplifiers together in parallel to increase RF power is phase matching within the amplifier channels. For a worst-case phase imbalance between MMIC amplifiers of ϕ, the combined voltage adds vectorially so the total normalized power of four amplifiers would be $4\cos^2\ \phi$. The power lost due to phase imbalance is $4(1-\cos^2\ \phi)$. Ideally, we would like each amplifier to have the same insertion phase. For each of the power amplifiers we purchased, Alpha Industries provided us with scattering parameters with which we determined the insertion phase for each amplifier. We carefully selected amplifiers to maintain a phase balance of ± 5 deg to keep this power loss less than 0.03 dB.

C. Power Dividers

The power combiners allow us to combine the power of the four relatively low-power devices to achieve the desired output power level, which is significantly higher than what can be obtained with a single device. The power divider requirements for this SSPA were small size (smaller than a waveguide), low loss (less than 1.2 dB), good phase match (less than 2 deg), and good port isolation (greater than 15 dB). Typical microstrip power combiners include tee dividers, branchline and ratrace couplers, Wilkinson dividers, and Gysel dividers. Wilkinson and Gysel dividers are the only type that provide both phase match and isolation. A Gysel divider is capable of handling higher RF power levels while maintaining phase match and isolation because the isolation resistors are positioned to provide a heat conduction path to the ground plane, whereas in the Wilkinson divider, they do not.

The initial power divider shown in Fig. 7 was designed using EEsof's Touchstone circuit analysis software. Like the Wilkinson, it divides the power through two 75-ohm quarter-wave sections. The two isolation resistors are joined into the remaining 75-ohm quarter-wave

ring through 100-ohm quarter-wave lines. Compensation for mismatches at the tee-junctions was incorporated into the geometry of the divider by using 30-deg notch cutouts [2]. A single two-way divider was fabricated at the David Sarnoff Hybrid Processing Facility. Thin-film deposition processes were used to fabricate the microstripline circuit and the thin-film isolation resistors onto the 0.25-mm (10-mil)-thick alumina substrates. The measured insertion loss, isolation, and phase match for the two-way divider were 0.5 dB, 12 dB, and 2 deg, respectively. The insertion loss is shown in Fig. 8. This circuit was also analyzed using finite difference time domain (FDTD), a full-wave analysis method for solving Maxwell's equations that include electromagnetic effects not accounted for in Touchstone's circuit simulator. FDTD analysis predicted a 0.4-dB insertion loss as compared to 0.2 dB on Touchstone (Fig. 9).

III. SSPA Integration

The SSPA was designed such that two separate amplifier modules, a preamplifier/driver module and an output module, could be tested and then dropped into a housing to be integrated with the input and output waveguide ports and bias supply connections.

A. Amplifier Modules

The amplifier modules consist of carriers that integrate the MMIC devices with passive transmission line circuits, RF decoupling capacitors, and dc bias ports. Molybdenum was selected as the carrier material because its thermal expansion coefficient is well matched to the alumina substrates mounted to it. In addition, molybdenum provides higher heat conduction for the thermal management of the power devices. Substrates and devices are mounted with conductive silver epoxy into recessed channels in the carrier, which helps suppress potential RF moding. Bias voltages are injected through the bottom of the carrier with miniature dc feed throughs. Two parallel bypass capacitors are located adjacent to the MMIC dc bonding pads. The small 0.6-pF bypass capacitors located closest to the MMIC device filter frequencies above 20 GHz, while the 100-pF capacitor provides higher-level bypassing at the lower frequencies. This filtering effect was modeled using EEsof's Touchstone and is shown in Fig. 10, where the filter response is shown with and without the 0.6-pF capacitor.

B. Housing

The SSPA housing was designed as a double-sided unit with two end pieces containing the waveguide ports. The preamplifier and output power amplifier modules are located on the top side of the housing (Fig. 11), and dc wiring from the Cannon-D connector to the miniature feed throughs on the modules are routed on the bottom side (Fig. 12). Large 0.1-μF ceramic bypass capacitors that stabilize the amplifiers against low-frequency oscillation are also located in the bottom compartment.

The end pieces are WR-28 waveguides incorporating E-plane waveguide probes. These probes are of the same design as those used in the DSS-13 experimental 32-GHz low-noise HEMT amplifiers. The probes are connected to the microstrip transmission lines via glass bead feed throughs (the same as those used in Wiltron's K-connectors) soldered into the housing. Figure 13 shows a cross-sectional view of the transition and E-plane probe assembly.

C. Thermal Issues

A thermal analysis was performed for the SSPA; it indicated that the maximum expected junction temperature for a 50 deg C baseplate (preliminary Pluto specification) would be 82 deg C provided that gold/tin eutectic solder is used to secure the MMICs to a molybdenum carrier. To speed up the assembly process time, we used conductive silver epoxy to secure the MMICs, bypass capacitors, and microstrip circuits. By using conductive epoxy, the thermal analysis predicted that the junction temperatures would change from 82 deg C to somewhere between 92–115 deg C depending upon the epoxy thickness and consistency. For our initial benchtop demonstration, the breadboard SSPA is held at room temperature (20 deg C), so the MMICs operate with junction temperatures of 62–85 deg C, and the use of silver epoxy is not a thermal concern. Typically, junction temperatures should be kept at or below 110 deg C for acceptable reliability in long-term spacecraft missions.

The thermal model used actual layout dimensions for all of the heat producing field effect transistors (FETs) within the MMICs placed on carriers within the housing. Table 2 shows the thermal conductivity values of the different materials used in the electronics package.

IV. SSPA Performance

The complete SSPA performance parameters are summarized in Table 3 and discussed in detail below. The test setup used for integration and test is shown in Fig. 14. In order to make the single-frequency (31.5-GHz) measurements to generate the compression curves (Figs. 15 and

16), the sweep oscillator source was used in conjunction with a power meter and calibrated waveguide coupler only.

Output power was measured to be 1.56 W with a corresponding power added efficiency of 15.4 percent. Figure 15 shows output power and power added efficiency plotted against input drive level. The amplifier was tuned to have maximum power at 31.5 GHz; however, it can be tuned for the same performance at 32 GHz.

Figure 16 shows SSPA gain and power added efficiency plotted against drive level. Note that in order to achieve the 1.5-W output power level, the SSPA is driven well into compression. The corresponding gain compression level at 1.5-W output power is 3.5 dB. At the maximum output power of 1.56 W, the corresponding compression level is 8.7 dB.

Figure 17 shows a swept frequency response from 27.5–37.5 GHz. As mentioned above, the peak power occurs at 31.5 GHz and is tunable from approximately 31–33 GHz by using gold ribbon stubs located on the power divider transmission lines. The active power devices (Alpha AA035P2-00) have power gain variations of ± 1.2 dB from 30–34 GHz, while the input and output power combiners have minimum insertion loss in this frequency region. The preamplifier (Alpha AA035P3-00) has consistent gain flatness from 30–36 GHz and does not affect the response as severely as the output devices. The input return loss was measured to be 19 dB looking into the input waveguide port. The output return loss was 12 dB and was measured at the output waveguide flange.

V. Summary

A solid-state power amplifier operating at 31.5 GHz with greater than 1.5 W total RF power and greater than 15 percent power added efficiency has been demonstrated using existing devices. Fabrication of the hardware provided valuable practical experience in the area of MMIC insertion. System-level issues for SSPAs were also addressed, including the impact of output losses on efficiency, phase matching within the parallel amplifier channels, bias circuit design, and system gain distribution.

Several areas have been identified for potential future work. The advanced high-power discrete devices from GE Aerospace (now Martin Marietta) having power added efficiencies of 30 percent have been integrated into an SSPA output module with an output power of 1.7 W (25 deg C), a corresponding power added efficiency of 27.8 percent, and an RF gain of 7.3 dB. A discrete preamplifier section could be designed to interface with this output module and boost the RF gain up to 32 dB with an efficiency of 27 percent. Additionally, in the near term, the SSPA described herein is being planned to be tested at low temperatures (−100 deg C) to study improved output power and efficiency behavior. This temperature range would be easily achieved using passive radiative technology on a spacecraft.

Acknowledgments

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References

[1] R. Knochel and B. Mayer, "Broadband Printed Circuit 0°/180° Couplers and High Power Inphase Power Dividers," *IEEE MTT-S Symposium Digest*, pp. 471–474, 1990.

[2] R. Chadha and K. C. Gupta, "Compensation of Discontinuities in Planar Transmission Lines," *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-30, no. 12, pp. 2151–2155, December 1982.

Table 1. SSPA gain distribution and predicted performance parameters.

Component	dc power consumption, W	Compressed gain, dB	Net gain, dB	Output power, dBm
Preamplifier	1.128	17.23	17.23	20.23
Driver amplifier	1.971	7.64	24.87	27.87
Two-way divider	0.000	−3.60	21.27	24.27
Two-way divider	0.000	−3.50	17.77	20.77
High-power amplifier	7.816	7.19	24.96	27.96
Two-way combiner	0.000	2.50	27.46	30.46
Two-way combiner	0.000	2.40	29.86	32.86
Waveguide transition	0.000	−0.25	29.61	32.61
Isolator	0.000	−0.15	29.46	32.46

Input parameters

Input power, 3.00 dBm
RF phase alignment, 10 deg

Calculated parameters

RF output power, 1.71 W
SSPA dc power, 10.92 W
SSPA efficiency, 15.66 percent

Table 2. Thermal conductivities used in thermal analysis calculations.

Material	Thermal conductivity, W/m-deg C
GaAs MMIC	44.1
AuSn eutectic solder	57.1
Silver epoxy	2.0–5.9
Molybdenum	133.8
Aluminum	157.4

Table 3. SSPA performance parameters.

Design parameter	Measurement
Output power, W	1.56
Power added efficiency, percent	15.4
Small signal gain, dB	42.7
Total dc power, W	10.1
Input return loss, dB	19
Output return loss, dB	12

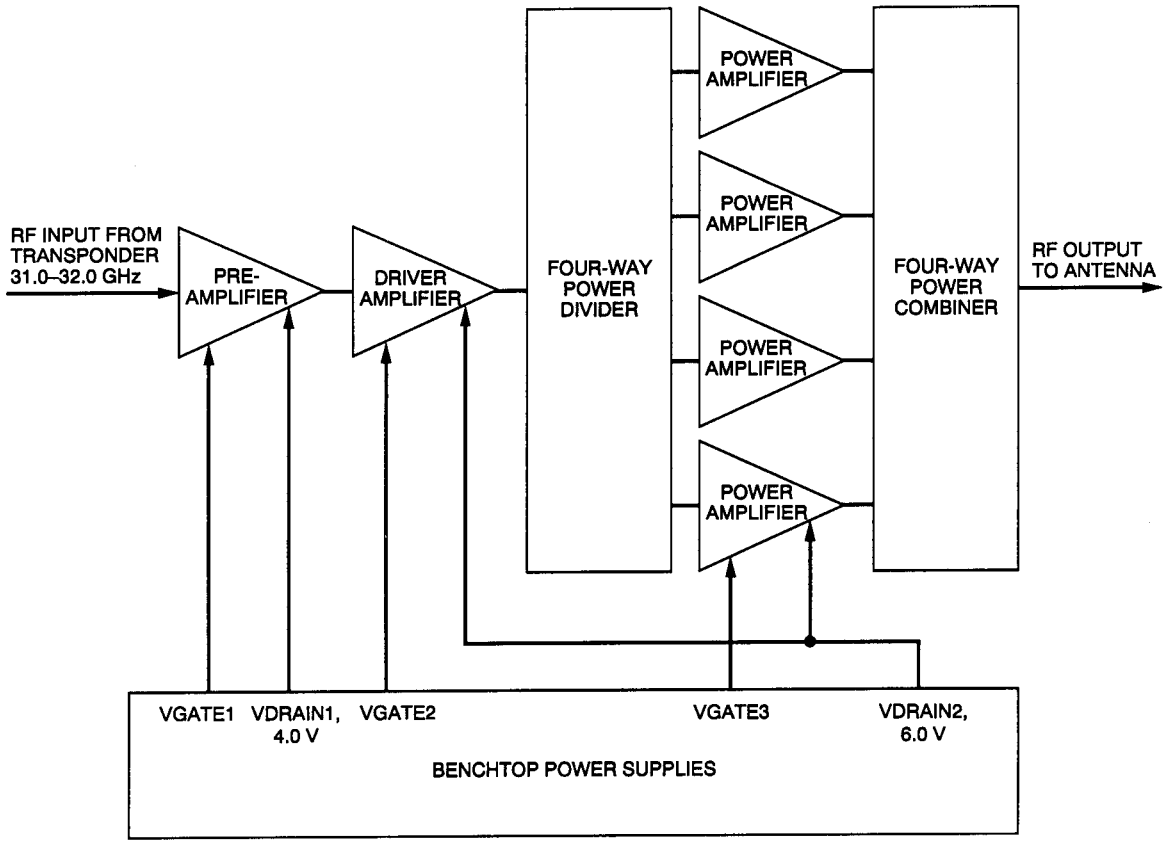

Fig. 1. The 32-GHz solid-state power amplifier.

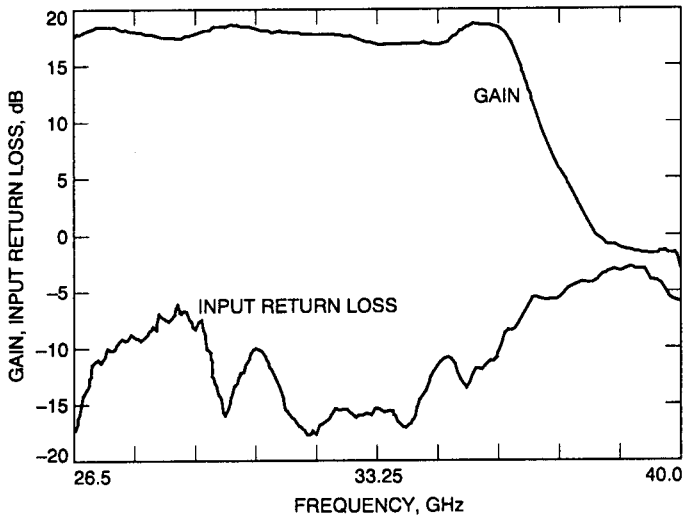

Fig. 2. Alpha MMIC preamplifier frequency response and return loss plots showing a 17.9-dB gain at 32 GHz and an associated return loss of 17 dB.

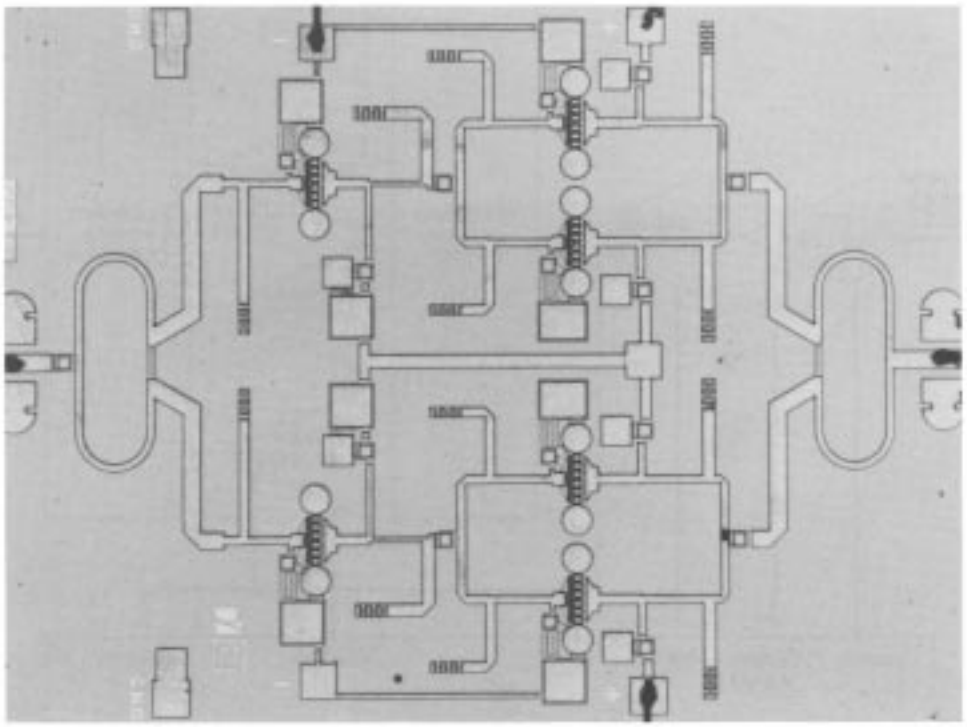

Fig. 3. Alpha 0.5-W MMIC power amplifier chip.

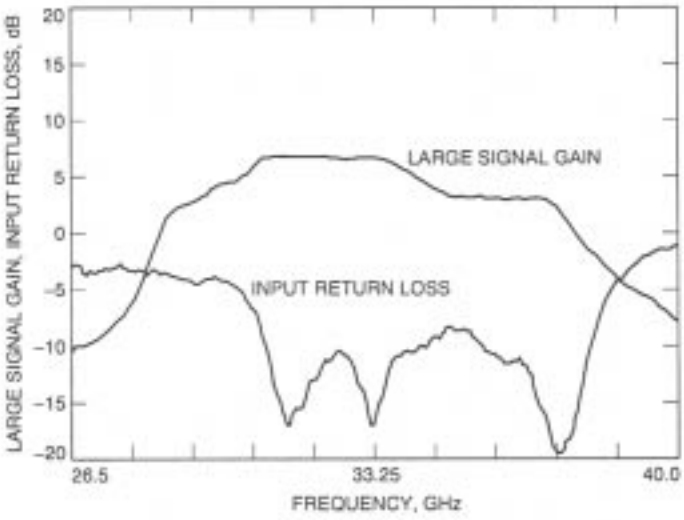

Fig. 4. Alpha MMIC power amplifier frequency response and return loss plot showing a 7.0-dB gain (compressed) at 32 GHz with an associated return loss of 12 dB.

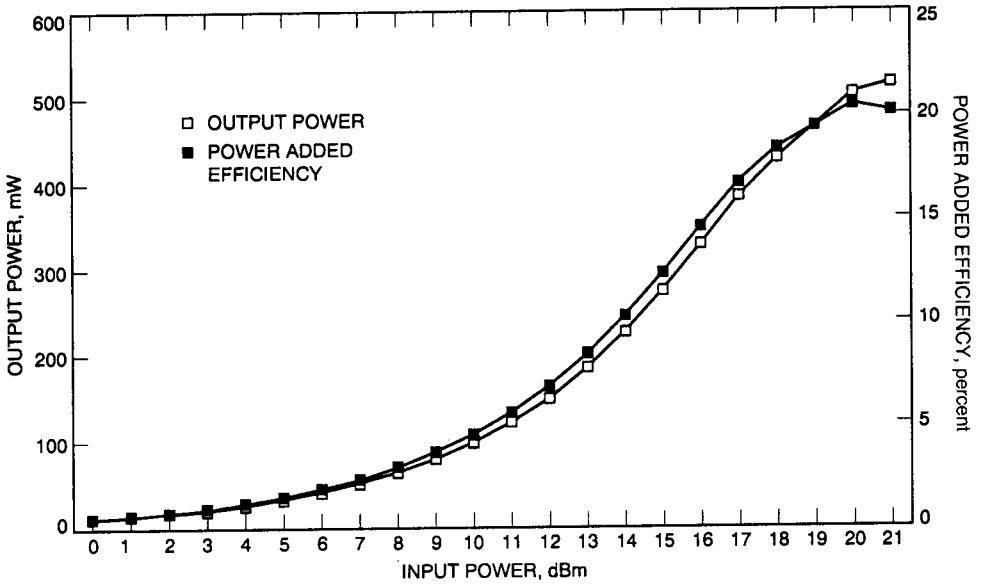

Fig. 5. Output power and power added efficiency plotted against input drive level for the Alpha MMIC power amplifier.

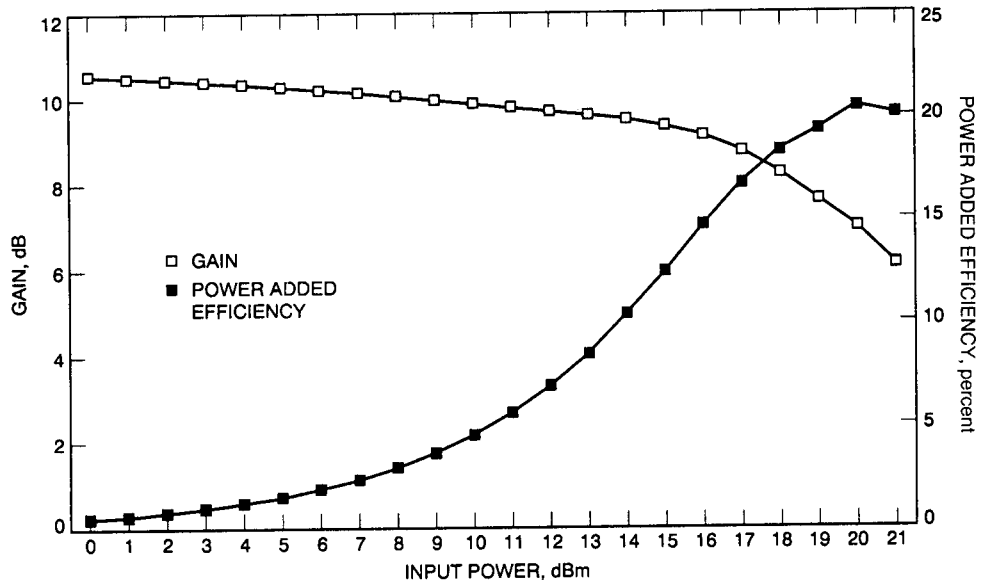

Fig. 6. Amplifier gain and power added efficiency plotted against input drive level for the Alpha MMIC power amplifier.

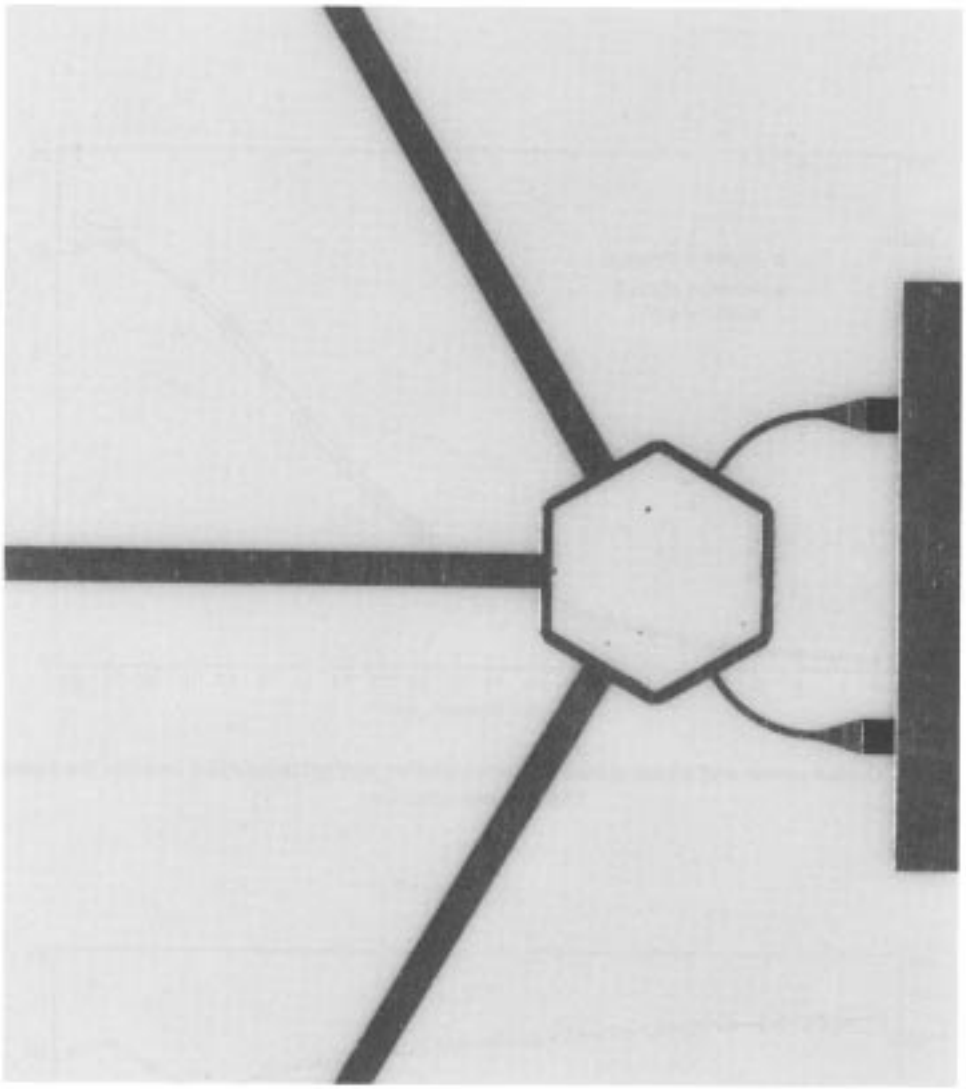

Fig. 7. The Gysel two-way power divider.

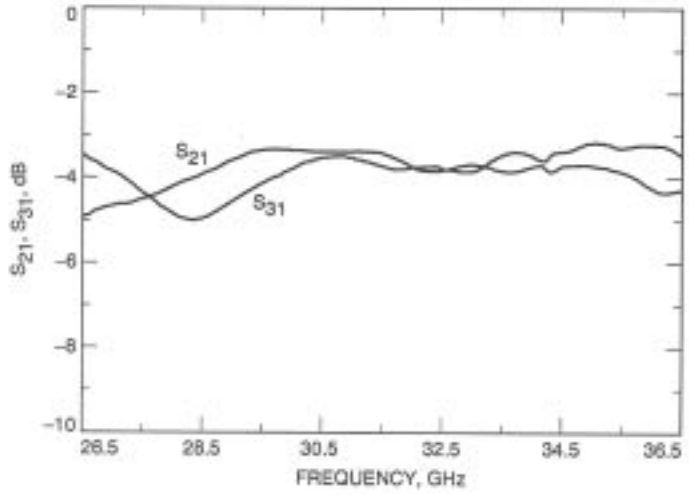

Fig. 8. Measured insertion loss of a two-way Gysel power divider.

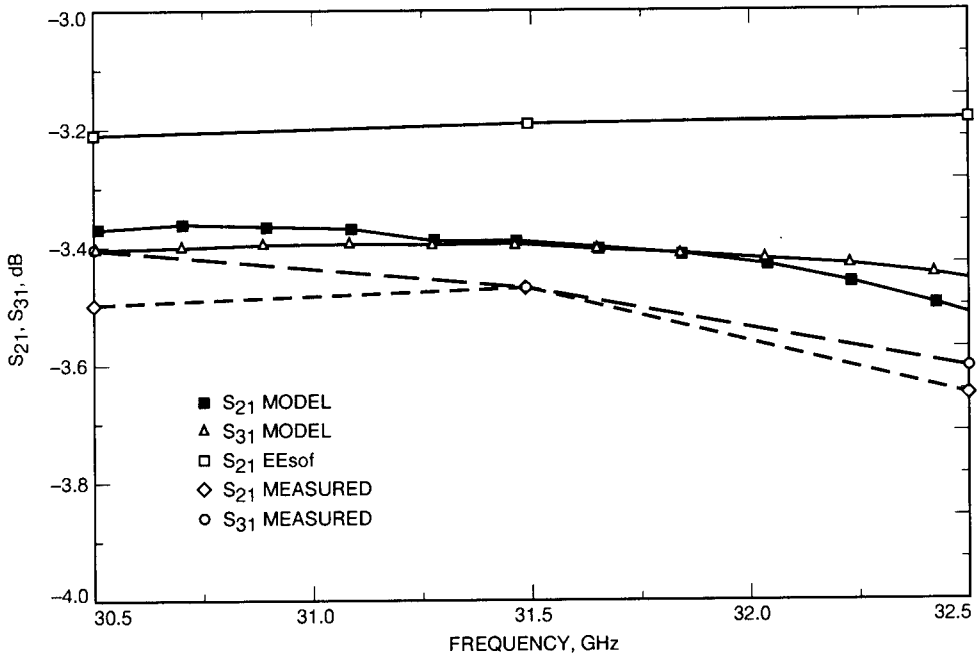

Fig. 9. Comparison between measured data, EEsof Touchstone model predictions, and FDTD model predictions for the Gysel two-way power divider. The FDTD model gave a more accurate insertion loss prediction.

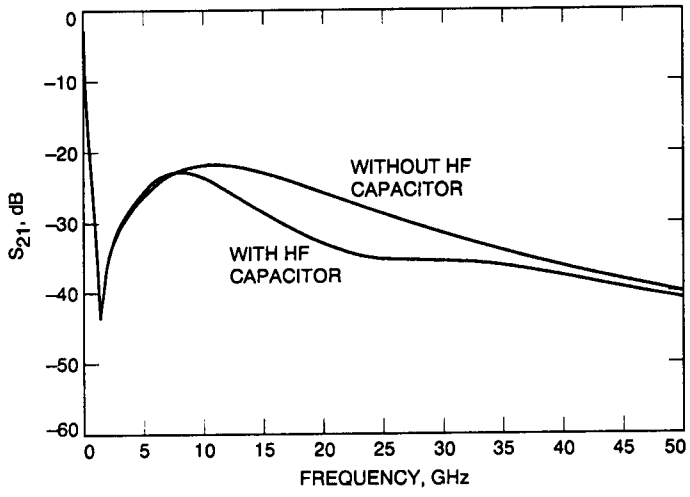

Fig. 10. The dc bypass filter response characteristics, showing the effect of adding a secondary 0.6-pF high-frequency (HF) capacitor in the network. An additional 5–10 dB of rejection is obtained between 10–37 GHz.

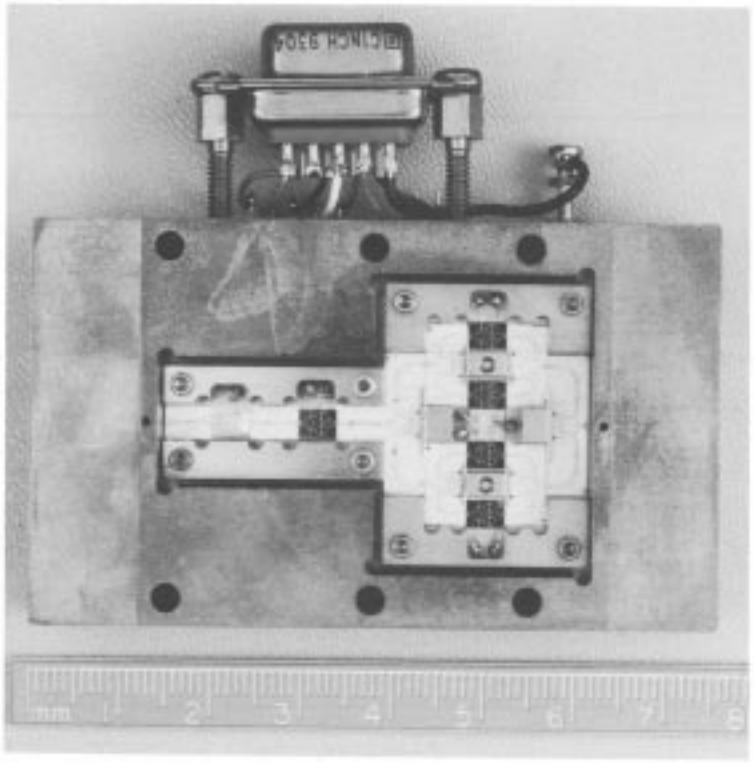

Fig. 11. Photograph of the 32-GHz SSPA showing the RF component side.

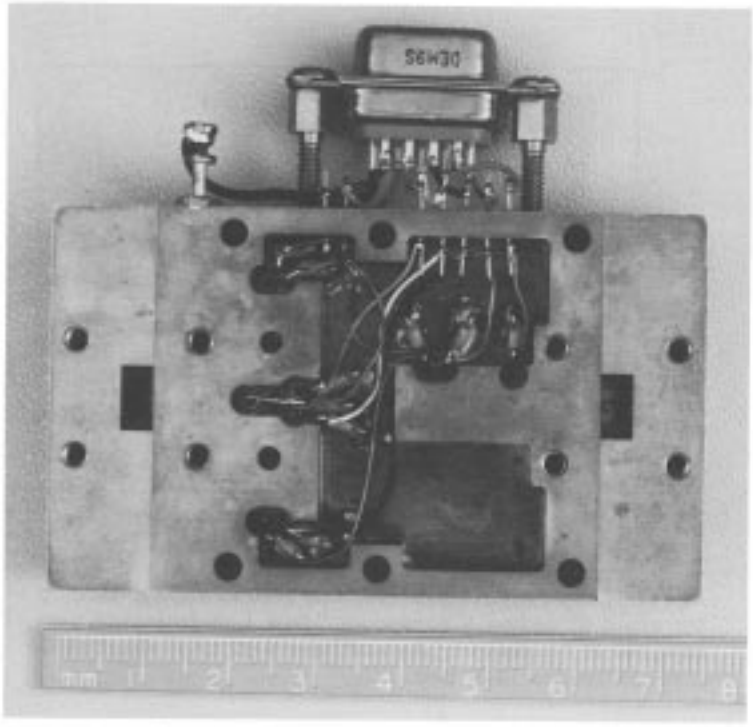

Fig. 12. Photograph of the 32-GHz SSPA showing the dc component side and the waveguide input and output ports.

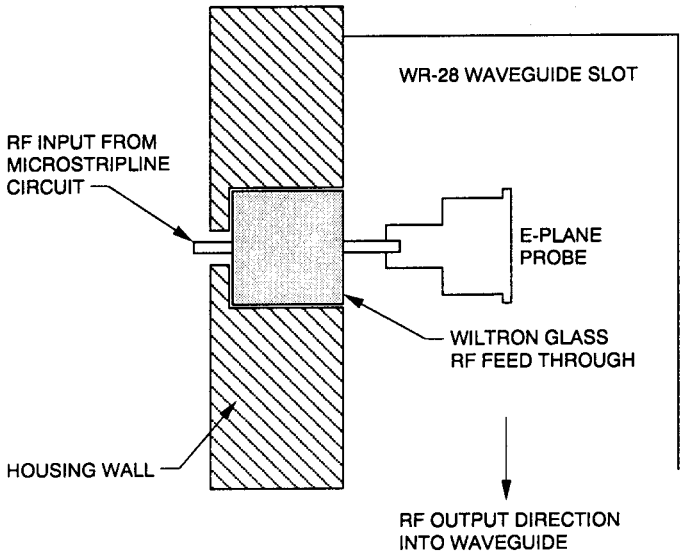

Fig. 13. E-plane microstrip-to-waveguide transition cross-sectional view.

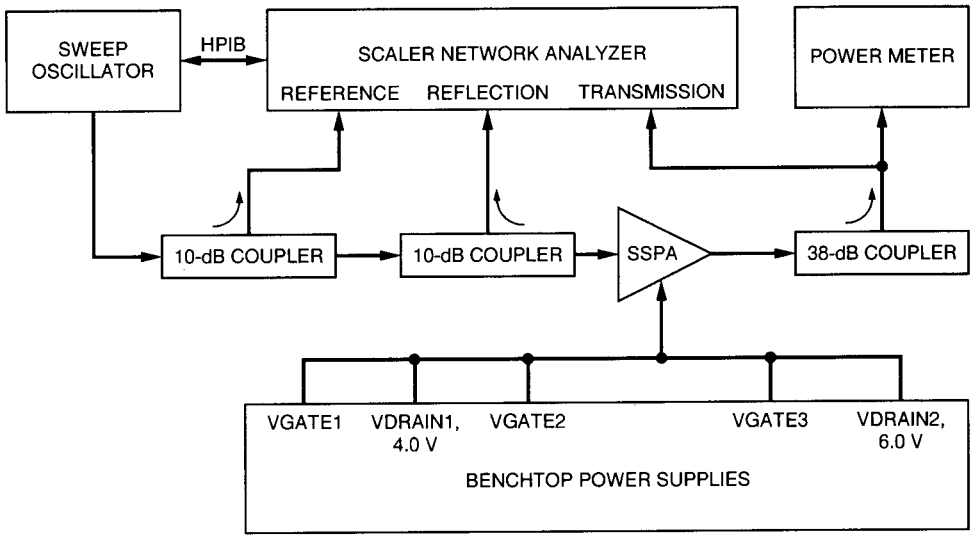

Fig. 14. The measurement system.

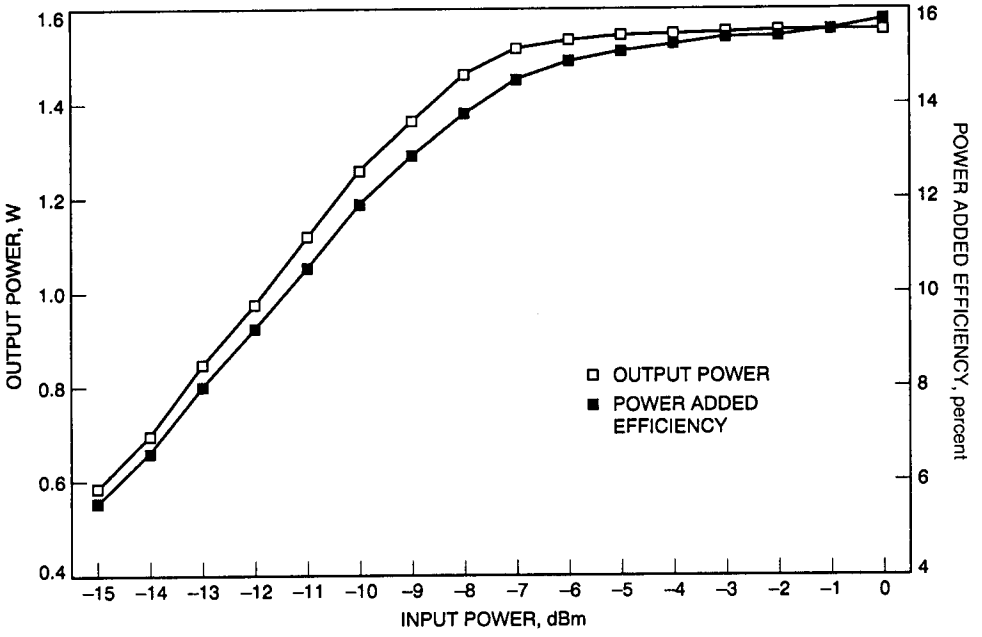

Fig. 15. Output power and power added efficiency plotted against input drive level for the 32-GHz SSPA.

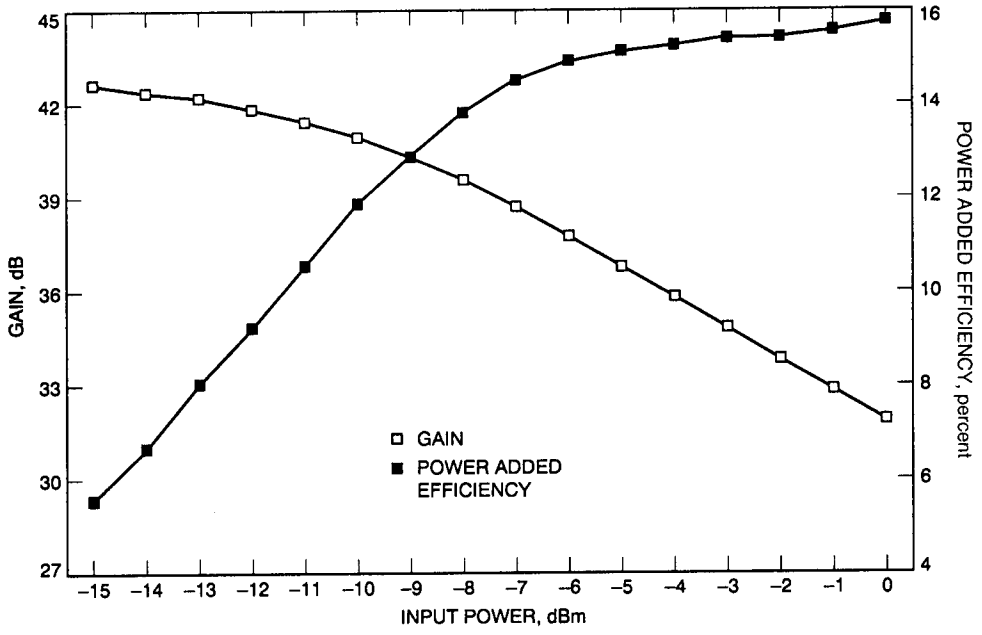

Fig. 16. Amplifier gain and power added efficiency plotted against input drive level for the 32-GHz SSPA.

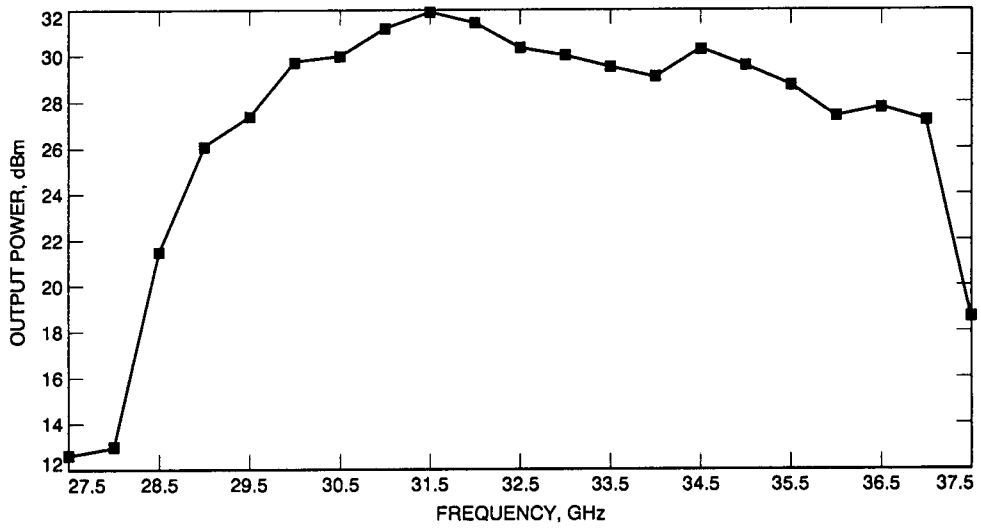

Fig. 17. Frequency response for the 32-GHz SSPA. The peak power was tuned at 31.5 GHz.