

GCF DSS Communications Equipment Subsystem High-Speed Data Assembly

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This article describes the functional operation of the Ground Communications Facility (GCF)-developed and supplied high-speed data assembly now in use at each Deep Space Station (DSS), except DSS 13 (Venus DSS), and CTA 21 (JPL Compatibility Test Area at Pasadena). The article discusses the subassemblies used, including those developed and incorporated during the latest reconfiguration, to fulfill the GCF High-Speed System requirements for the 1971-1972 period. The assembly is used to convert all high-speed data leaving the DSS to a form suitable for transmission to the Space Flight Operations Facility and converts all high-speed data entering the DSS to a form suitable for use by the on-station computers.

I. Introduction

This article discusses the functional operation of the major subassemblies (Fig. 1) making up the 1971-1972 configuration of the Ground Communications Facility (GCF)-DSS Communications Equipment Subsystem (DCES)-High-Speed Data Assembly (HSDA). This article will also briefly note the changes made to the pre-1971-1972 configuration of the DCES-HSDA described in Ref. 1 and implemented in accordance with System Design information contained in Refs. 2 and 3 and the Evans article¹ in this issue.

¹Evans, R. H., "GCF High-Speed Data System Design and Implementation for 1971-1972" (this issue).

II. Purpose of DCES-HSDA

The DCES-HSDA selects data from the Deep Space Instrumentation Facility (DSIF) on-station computers (OSC) and converts them to a form suitable for transmission to the Space Flight Operations Facility (SFOF). It also converts the data transmitted from the SFOF to a form suitable for use by the OSCs and distributes the data to the appropriate OSCs.

The transmission portion of the DCES-HSDA provides automatic priority selection of transmission from a maximum of four OSCs, continuous data transmission by the automatic addition of filler data, block error

detection encoding, and the conversion of digital data blocks to a form suitable for transmission to the SFOF.

The receive portion of the DCES-HSDA provides the conversion of the voice band data from the SFOF to digital data, block error detection decoding, and the inspection of the User Dependent Type (UDT) code of the received data to determine the appropriate distribution of received data to any combination of up to six OSCs.

The information transmitted and received by the DCES-HSDA is organized in standard message segments of 1200-bit data blocks. Each data block consists of a header, data, and an ending (see Fig. 2).

- (1) The header, provided by the data source, is 120 bits long and is represented by lines 1 through 5 of Fig. 2. The sync code is bits 1 through 24. The source code, bits 25 through 32, identifies the transmitting station. The destination code is bits 33 through 40. The block format code, bits 41 through 48, identifies block size and whether the block contains computer-generated data or block multiplexer (BMXR)-generated filler data. The UDT, bits 52 through 58, is inspected by the block demultiplexer (BDXR) to determine the distribution of received data to OSCs.

The rest of the header, provided for data user only, is self explanatory except for the Multiple Mission Support Area (MMSA) code bits 97-98. The MMSA code is used to identify the tracking station in those instances where data blocks transmitted from any given tracking station contain data received from a spacecraft being tracked by another station.

- (2) The data section contains 1044 bits. The data section may be computer-generated data or filler or test data from the BMXR.
- (3) The ending is the last 36 bits, prepared and added by the encoder before transmission. The ending contains the 3-bit error status code and the 33-bit error control code. The decoder inspects each received data block and changes the three error status bits to ones if no error is detected.

For purposes of the ensuing discussion transmitted data (SD) will be followed from a DSIF OSC through the DCES-HSDA and received data (RD) through the DCES-HSDA into the DSIF OSCs. The DCES-HSDA now consists of three equipment racks, one of

which was added in 1970 as described by Evans (Footnote 1).

III. Transmitted Data Flow Through the DCES-HSDA

A. Data Source

Up to four OSCs may initiate request-to-send (RS) control signals to the BMXR when they are ready to transmit data to the SFOF. When the BMXR is ready to pass data, it will initiate a clear-to-send signal to the highest priority OSC with its RS signal on. One bit time later that OSC must begin transfer of its 1164-bit data block. The transmitting OSC must turn off its RS immediately after bit time 1164 for at least one bit time.

B. Block Multiplexer Switch and Test Panel

Data from an OSC enters the BMXR switch and test panel (switch) where it is routed to one of two BMXRs. The BMXR switch provides for independent switching of data, control and timing signals between four OSCs and the two BMXRs. The switching is not operationally done on an individual basis however. Only one channel, prime or backup, may have access to the one HSD line to SFOF (Ref. 2) so all four OSCs are always switched to access the same BMXR via the BMXR switch.

In the pre-1971-1972 configuration of the DCES-HSDA, the BMXR switch and BMXRs also passed received data from SFOF to all four OSC inputs. That functional requirement is now obsoleted with the addition of the BDXRs as discussed in Ref. 4.

C. Block Multiplexer

The SD flow from the BMXR is continuous block formatted data selected on a priority basis from up to four OSCs or from the BMXR's internal preprogrammed filler block generator. The priority order of transmission from the OSCs through the BMXR is established by the setting of the priority switches on the BMXR.

At bit time zero the BMXR will begin transfer of a data block to the encoder. At the time the 1164th bit is received in the encoder, the encoder will turn off its clear-to-send (CS) signal to the BMXR. At the same time the transmitting source (OSC) must turn off its RS signal for at least one bit time and the BMXR begins its search for the source of the next data block. If the transmitting source of the last data block turns its RS

signal on before bit time 1198, the BMXR will consider its priority in the selection of a source for the next data block. At bit time 1198 the BMXR makes its selection. At bit time 1199 the encoder turns on the CS signal, and at bit time zero the selected source will begin sending its 1164-bit data block. If no OSC has its RS signal on at bit time 1198, when the BMXR is making the source selection, the BMXR will select its own filler block generator as a source of the next data block, thereby retaining continuous data transmission. The filler block generator is always the lowest priority selection of the BMXR.

D. Encoder

The encoder monitors and controls the flow of digital data from the OSCs going to the data set. Normal operation begins when the encoder receives an RS signal from the BMXR. The encoder then turns on and controls an RS signal to the data set. If the data set is ready, it will send a CS signal to the encoder. The encoder then completes the loop by turning on its CS signal to the BMXR. One bit time later the BMXR-selected data source will begin transfer of 1164 bits of data and the encoding process begins as described in Ref. 1. As the encoder receives the 1164th bit, it turns off the CS signal to the BMXR. As long as the DCES-HSDA is operating normally, the encoder will keep an RS signal to the data set turned on and the data set will keep its CS signal to the encoder turned on.

The encoder completes its processing of a data block by inserting three *zero* bits (the error status code) followed by the 33-bit error detection pattern as the data flows through the encoder from the BMXR to the data set. The encoder delays SD only one bit time in performing its encoding function.

E. Data Set Transmitter

The transmitter portion of the newly implemented Western Electric Co. 203A (4800 bps) full-duplex data set discussed by Evans (Footnote 1) is used primarily to convert encoded digital data input to an amplitude-modulated vestigial sideband voice frequency signal suitable for transmission to the SFOF via a standard voice frequency channel meeting American Telephone and Telegraph Co. specifications for a C2 grade transmission circuit. The data set also determines the bit rate and provides for synchronous transmission of data by providing the SD timing signal, Serial Clock Transmit (SCT), to the encoder, BMXR, and OSCs.

F. Data Set Control Panel

The new Data Set Control Panel (DSCP) discussed by Evans (Footnote 1) was designed and added to provide the operator with the required visual status indicators and a means to initiate a manual retrain of the associated 203A data sets.

G. Data Set Interface Module

The Data Set Interface Module (DSIM) was designed and added to provide a connector interface point between the prime and backup data sets and the audio frequency (AF) patch panel where the DCES-HSDA interfaces the one HSD line to the SFOF. The line input/output of the prime data set is normalled through the AF patch panel to the HSD line. If the operator wishes to place the backup data set on line, he must insert patchcords in the AF patch panel. The DSIM was equipped with attenuators to assure the proper signal levels at the DCES-HSDA interface with the transmission line to the SFOF.

IV. Received Data Flow Through the DCES-HSDA

A. Data Set Receiver

The receiver portion of the full-duplex data set discussed by Evans (Footnote 1) converts the amplitude modulated vestigial sideband voice frequency signal from the SFOF to serial digital data and routes it to the decoder. Under normal operating conditions a data block leaving the data set receiver will be exactly the same as it was as it left the encoder and entered the data set transmitter. The data set receiver also recovers an RD timing signal from the incoming data and routes it to the decoder, BDXR, and OSC as the Serial Clock Receive (SCR) signal.

B. Decoder

The decoder receives the incoming data blocks, via the interface buffers, and delays the data 1201 bits while it examines their validity as discussed in Ref. 1. The decoder then labels each error-free block by setting the three error status bits to 1's in accordance with Footnote 1 and forwards the data block to the BDXR.

C. BDXR and BDXR Patch and Test Panel

The BDXR and BDXR patch and test panel described in Ref. 3 were designed and added to direct each RD block only to the OSCs addressed in that data

block. The BDXR checks the UDT code information in bits 52 through 58 of each RD block and distributes the block accordingly.

The necessity for the addition of this demultiplexing capability was brought about by the increase in volume of received data and the change in data rate (from 2400 to 4800 bps) as explained in Ref. 4 and Footnote 1.

V. Data Flow Monitoring

Inputs and outputs of each subassembly are normalled through either the AF Patch and Test Jackfield, the DC Patch and Test Jackfield, the BMXR Switch and Test Jackpanel or the BDXR Patch and Test Panel. Signals passing between subassemblies may be monitored at one of the above-mentioned jackfields without interrupting data flow. When one of the visual status indicators on a subassembly signifies the presence of an abnormal condition, the operator may quickly isolate the anomaly and substitute, by using patchcords or switches, any or all backup subassemblies as required to restore normal operation. The DCES-HSDA also provides selected monitor signals for use in the monitor program. In general, the signals provide information on the configuration, mode of operation, and status of the subassemblies in use.

VI. Summary

The ten DCES-HSDAs located at CTA 21 and all DSSs (except DSS 13) have been upgraded as follows to meet the 1971-1972 HSS requirements:

- (1) The Western Electric Co. (WECO) 205B (2400 bps) data sets were replaced with NASCOM-provided WECO 203A (4800 bps) data sets.
- (2) Data Set Control Panels were designed and incorporated to provide the operator with a means of controlling the operation of the 203A data set and observing its status.
- (3) Data Set Interface Modules were designed and incorporated to provide a connector interface for the 203A data sets and transmit/receive line level control.
- (4) Block Demultiplexers (BDXR) were designed and incorporated to provide discriminate distribution of received data blocks to on-station computers (OSCs). The Block Demultiplexer Patch and test panels were designed to provide the necessary patch and test capability between the BDXR and OSCs.
- (5) Two existing equipment racks were rewired and reconfigured, and one new rack was designed and added, to accommodate the new subassemblies added to the DCES-HSDA.

References

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2. McClure, J. P., "Ground Communications Facility Functional Design for 1971-1972," in *The Deep Space Network*, Space Programs Summary 37-66, Vol. II, pp. 99-102. Jet Propulsion Laboratory, Pasadena, Calif., Nov. 30, 1970.
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4. Evans, R. H., "High-Speed Data Block Demultiplexer," in *The Deep Space Network*, Space Programs Summary 37-66, Vol. II, pp. 105-106. Jet Propulsion Laboratory, Pasadena, Calif., Nov. 30, 1970.

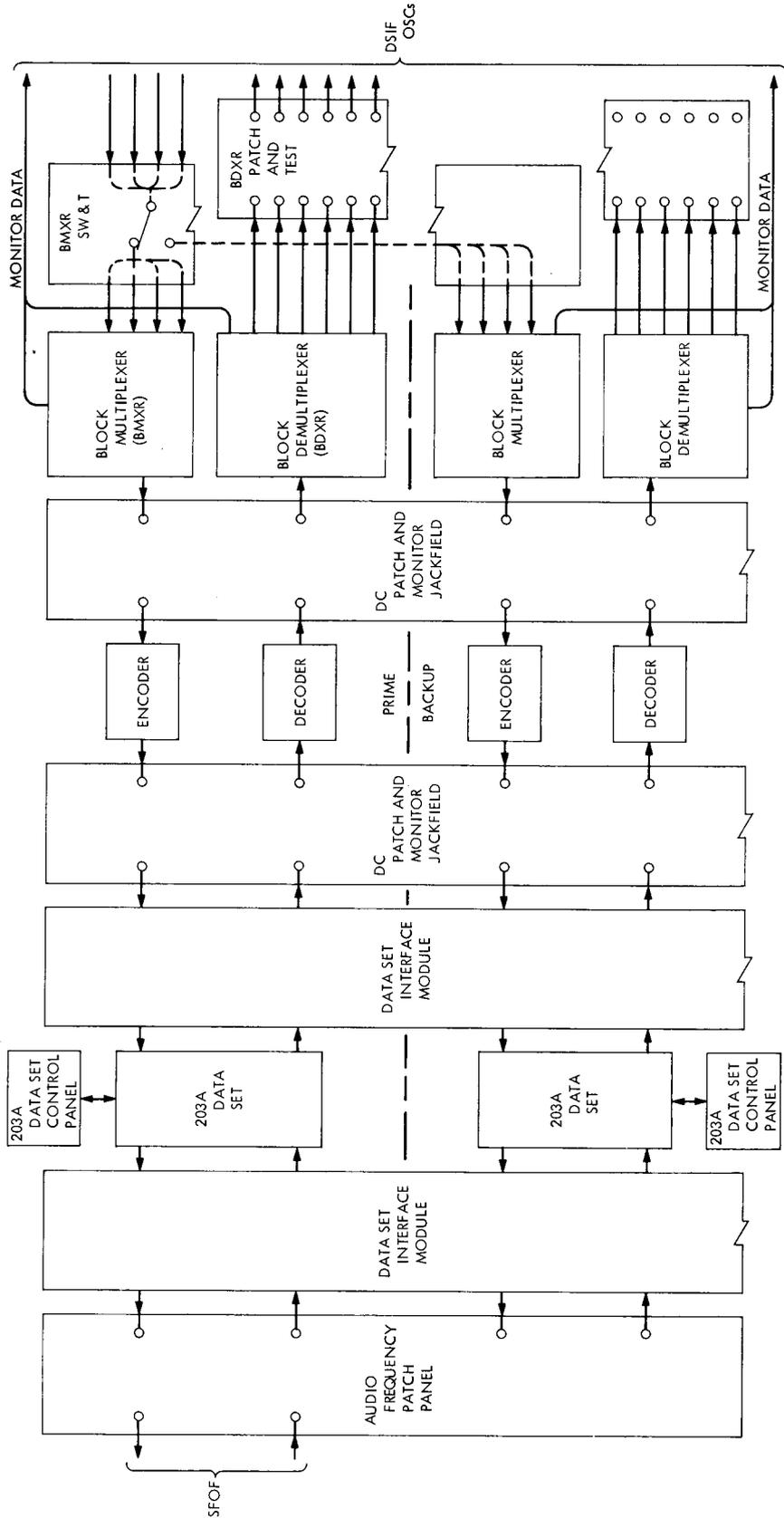


Fig. 1. DCES-HSDA functional block diagram 1971-1972 configuration

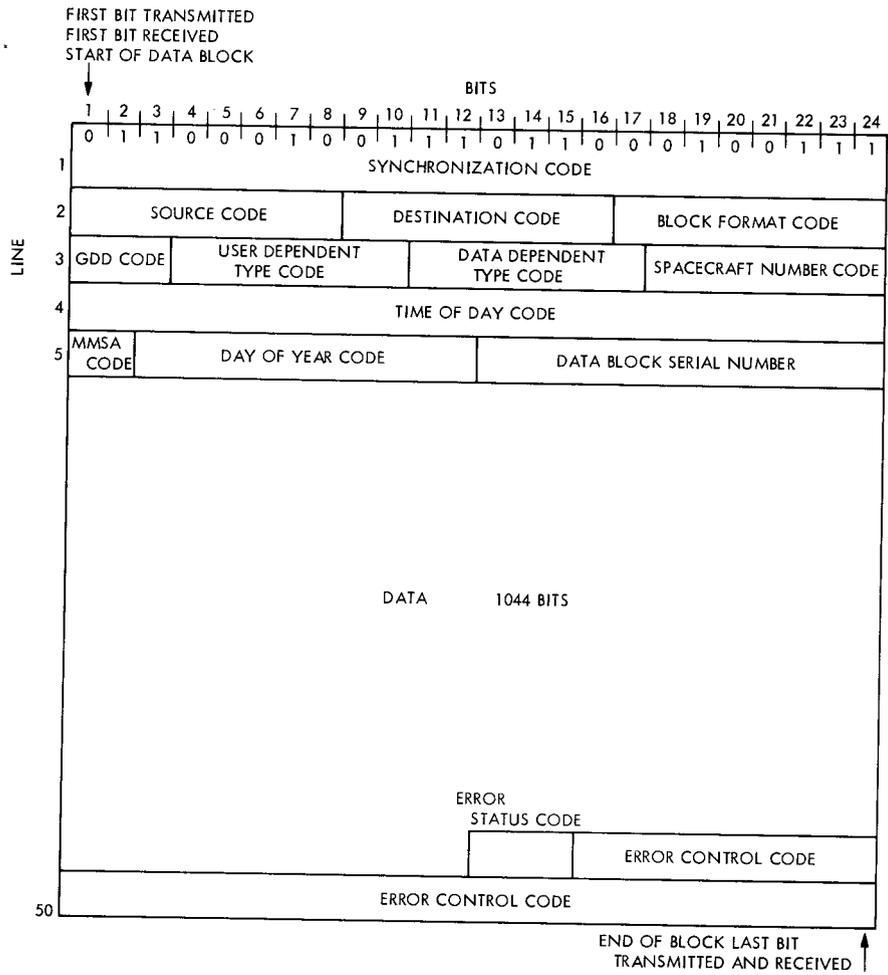


Fig. 2. Data block format